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·	Application No.	Applicant(s)
Notice of Allowability	10/692,383	TAKAHASHI, HIROYUKI
	Examiner	Art Unit
	ANH PHUNG	2824
	ANTIPHONG	2024
The MAILING DATE of this communication apperature All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this agor other appropriate communication GHTS. This application is subject	pplication. If not included on will be mailed in due course. THIS
1. This communication is responsive to the Election received on 12/30/04 & Telephone Interview on 3/7/05.		
2. The allowed claim(s) is/are <u>1-26,33,35,41 and 46</u> .		
3. The drawings filed on 23 October 2003 are accepted by the Examiner.		
 4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some* c) None of the: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this national stage application from the 		
International Bureau (PCT Rule 17.2(a)). * Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE. 5. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give	IENT of this application. itted. Note the attached EXAMINE	R'S AMENDMENT or NOTICE OF
6. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.		
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached		
1) ☐ hereto or 2) ☐ to Paper No./Mail Date		
(b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date		
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t		
7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
Attachment(s)	_	
1. Notice of References Cited (PTO-892)		Patent Application (PTO-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. ⊠ Interview Summar Paper No./Mail D	
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 10/23/03		
4. Examiner's Comment Regarding Requirement for Deposit		nent of Reasons for Allowance
of Biological Material	9. Ø Other <u>Search</u>	Phung
		HUNG EXAMINER

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Examiner's amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CAR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Donald W. Muirhead on March 7, 2005.

In the claims:

Cancel non-elected claims 27-32, 34, 36-40, and 42-45.

The examiner's amendment has been made in order to place the application in a condition for allowance.

2. Per telephone interview with Mr. Donald W. Muirhead, the non-elected claims 27-32, 34, 36-40, and 42-45 are cancelled per Examiner's amendment above, and the elected claims 1-26, 33, 35, 41 and 46 are pending in the application.

Information Disclosure Statement

This office acknowledges receipt of the following items from the Applicant:
 Information Disclosure Statement (IDS) filed October 23, 2003.
 Information disclosed and listed on PTO 1449(s) was considered.

Examiner's Statement of Reasons for Allowance

4. Claims **1-26**, **33**, **35**, **41** and **46** are allowed.

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Arimoto et al. (US 6,744,684), Matsuzaki (US 6,636,449) and Chun (US 6,166,980) disclose a semiconductor memory device having a refresh circuit similar to that of the present application, but fail to teach:

"a control unit for performing control so that when a mismatch is detected as a result of the determination by said first determination circuit, the read or write operation and a refresh operation are performed in parallel, wherein the read or write operation is performed using the word line and the bit line for one of said read and write systems for the memory cell selected by the read or write address signal, while the refresh operation is performed using the word line and the bit line for the other of said read and write systems for the memory cell selected by the refresh address signal and a sense amplifier for the other of said read and write systems, and when the match is detected as the result of the determination by said first determination circuit, the refresh operation is inhibited and the read or write operation using the word line and the bit line for said one of said read and write systems for the memory cell selected by the read or write address signal is performed" as claimed in the independent claim 1; or

"a control unit for performing control so that when a mismatch is detected as a result of the determination by said first determination circuit, a write operation and a refresh operation are performed in parallel, wherein the write operation is performed using the word line and the bit line for a write system for the memory cell selected by the address signal for write, while the refresh operation is performed using the word line and the bit line for a read system for the memory cell selected by the refresh address and a sense amplifier for a read system, and when the match is detected as the result

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of the determination by said first determination circuit, the refresh operation is inhibited, and the write operation is performed" as claimed in the independent claim 2; or

"an address comparator, receiving the refresh address signal output from the refresh address generator with the input address signal held in the address register for comparing the refresh address signal with the input address signal to output a comparison result indicating whether there is a match between the refresh address signal and the input address signal or not; and a second control circuit for performing control so that refresh operation as to the dual port memory cell associated with the refresh address signal and a read or write operation as to the dual port memory cell associated with the input address signal are executed in parallel, when the comparison result output from the comparator indicates a mismatch between the refresh address signal and the address signal held in the address register" as claimed in the independent claim 33; or

"storing and holding an externally input address in address holding circuit; comparing a refresh address output from refresh address generation circuit with the address held in said address holding circuit; performing control so that when the comparison result indicates that the refresh address does not match the address, a read or write operation using one of the ports for the write and read systems of selected one of said DRAM cells and a refresh operation using the other of the ports for the write and read systems are performed in parallel; and performing control so that when the comparison result indicates that the refresh address matches the address, the refresh operation is stopped" as claimed in the independent claim 41; or.

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"a control circuit for performing control so that, when the comparison result indicates that the refresh address signal does not match the input address signal, a read or write operation using one of the two ports of the cell associated with said input address signal and a refresh operation using the other of the two ports of the cell associated with said refresh address signal are performed in parallel" as claimed in the independent claim 46.

Any comments considered necessary by applicants must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comment on Statement of Reasons for Allowance".

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **ANH PHUNG** whose telephone number is **(571) 272-1883**. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD ELMS, can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

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Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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ANH PHUNG PRIMARY EXAMINER

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